all decoupling caps as close as pins as possible! PMID cap is the most critical. You can add additional small 0.01-0.1uF closest possible stereo audio input AudiolN 2 Top layer input capacitor: X5R or X7R ceramic capacitor placed as close PVDD ⊋ VREF as possible to the VIN and PGND -OUT\_₹ IN\_L VDD PGND MUTE active LOW MUTE\_LOW +OUT\_R (switch to GND) آ 10ر 6 output rapacitors very close to L2 and PGND PSU for eDP lane LCD C5 Figure 46. Layout Example Diagram C7 C9 Simple PSU input selection method for buck (from higher to lower voltage): 10uE12 EN PGND - adapter plugged in - highest priority audio amp powered from VSYS Resistor selection: - USB source plugged in - when adapter has no voltage  $R2 = 180 k\Omega$ - 1.8 V - R1 = 470 KΩ - 2.5 V - R1 = 750 kΩ - 3.3 V - R1 = 1 MΩ - battery only - when no other source USB OTG mode is boost mode; inductors. - delivers power from battery to USB host CoilCraft XFL4020-152ME Q: how to distinguish VBUS delivering power to host?  $-> 5V -> R1 = 1.6M \Omega$ Murata FDV0530S-H-1R5M D3 RBR5LAM40 (BUS (buck mode) calc: 3.9 - 17V adapter 3-54AD2  $R1 = (Vout/Vfb - 1) \times R2$ 3.5V – 4.35V —VSYS Vfh = 500mV10E R2=R1/(Vout/Vfb - 1)<- USB OTG 1.3A J11 1 CPSU1 IIuF (boost mode) PGND> 10 VIN PS630 VOUT J5 USB\_A\_female RBR5LAM40A USB OTG female 10uE12 EN U3 **■**VBUS PSØSÄNG END VRIIS PGND PSU for CPU, GPU, etc -> 3.3V or 5V D5 14 PSØSATNE ZNB 14 PSØS G G G W MM 2 NB 14 PSØS G G G W MM 2 NB 15 NB SYS PSEL -> D+(USB) 15 B024-195 /PG -> D - (USB) STAT SYS power good led not be higher than 0.22 μF SCL BAT 5.12V: R2=108K (180K || 270K) SFI ─ 15 LiPo 4.9V: R2=110K (180K | 300K) BAT\_CHGR\_INT INT is data output for host ∠OK} TPS63020 2-3A buck boost converter USB power USB on-the-go BAT CHGR OTG THERMISTOR(103-AT)1 cannot be paralleled directly! Use diode summer bank source ≺ thermistor SW PST SW CE - charge enable = active low Vin:2.5 V to 5.5 V Vout: 5.5V max host (promicro) DSJ Package 14-Pin VSON with Exposed Thermal Pad Output currents can go to 2 A in boost mode and to 4 A in buck mode Texas Instruments BQ24193 PSEL, OTG pins relate to 1.5A 5V USB adapter 4.00 mm x 4.00 mm QFN-24 Package If the portable device is attached to a charging port, High Efficiency 4.5-A Switch Mode Charger it is allowed to draw up to 1.5 A (with PSEL to OV) The bq24193 sets input current limit through PSEL and OTG pins. Input Current Limit: 100 mA, 150 mA, 500 mA, If PSEL pin is LOW limit is 3A. 900 mA. 1.2 A. 1.5 A. 2 A and 3 A ILIM resistor: 265 for 2A max • 3.9-V to 17-V Input Operating Voltage Range (12V / 4A) 357 for 1.5A max - supports all kinds of adapter with Input Voltage DPM Regulation - this is default buck mode After the input current limit is set, the converter is enabled and the HSFET and LSFET (between VBUS via PMID as input • USB OTG 5 V at 1.3 A Synchronous Boost Converter Operation at VBUS and SW as output) VSYS and PGND start switching. - this is boost mode -> OTG If battery charging is disabled, BATFET turns off. In Battery mode REGN stays off to minimize the quiescent current. Otherwise, BATFET stays on to charge the battery. Battery powers VSYS via internal BATFET switched on. When the DC source plugs in, the bg24193 checks the input source voltage Power Supply Unit with battery charger, PSEL: Power source selection input. High indicates USB host source to turn on REGN LDO and all the bias circuits. It also checks the input and Low indicates an adapter source. INT: open-drain Interrupt Output. The INT pin sends active low, double fixed voltage buck/ boost units current limit before starts the buck converter. 256-us pulse to host to report charger device status and fault. The REGN LDO supplies internal bias circuits as well as the HSFET OTG: USB current limit selection pin during buck mode, and and stereo power amplifier and LSFET gate drive. active high enable pin during boost mode. The LDO also provides bias rail to TS1/TS2 external resistors. /PG — power good (low means OK — green led on) STAT — status led (high means OK — red led off) The pull-up rail of STAT can be connected to REGN as well. File: BalthazarPSU.sch Title: Size: A4 Date: Rev: KiCad E.D.A. kicad (5.1.5)-3 ld: 1/1